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# Design of Arithmetic Unit Using 32-Nm CNFET Technology

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**ABSTRACT**
The main aims of the electronic manufacturing are miniaturization and make small size products. Recently we are using carbon nano tube field effect transistor (CNFET), which has short channel effect. CNFET is better than CMOS and FinFET technologies. [3]. In this project Arithmetic and Logic Unit is designed in CNFET 32 nm technology and analyze the power dissipation.
***Keywords:*** 4 bit Full Adder, CNFET, FinFET, CMOS, Power dissipation and Delay, ALU.

## I. INTRODUCTION

Electronic researchers are searching possible device for semiconductor industry for best performance. One of the most popular technologies is CNTFET technology which is used in microprocessors and application specific integrated circuits.

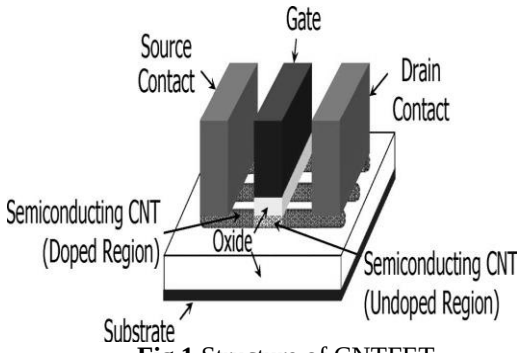


**Fig 1** Structure of CNTFET

The CNFET are used in make of logic circuits. It has low resistance and strong interconnects. This paper presents the following sections. Part I provides introduction, Part II provides about CNTFET technology, Part III provides design of logic gates, Part IV provides design of ALU circuits and Part V carries conclusion and future work.

## II. CNTFET TECHNOLOGY

Graphite sheets are rolled into tubs, which is called carbon nano tube. Carbon nano tube field effect transistors are high performance transistors [4].The carbon nano tubes was invented by SumioIijima of NEC Crop in Tokyo. He discovered carbon nano tubes in 1991.

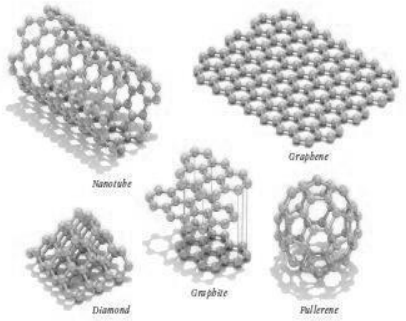


**Fig 2** Ideal CNTFET Technology Structure

### 2.1. TYPES OF CNTFET

Depending on the chirality, carbon nano tubes are classified into two types. They are single wall carbon nano tubes and multi wall carbon nanotubes. Single wall nano tube is created by a one layer of graphite sheet and multi wall carbon nano tube is made up by multiple layers.

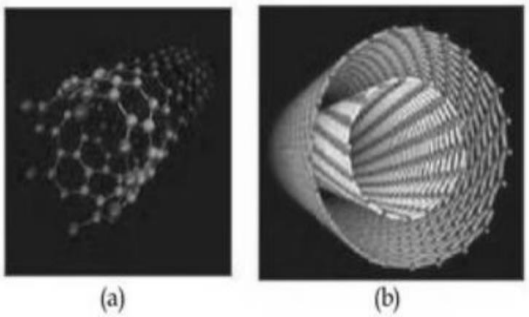


**Fig: 3** Structure of nanotubes **(a)** SWCNT **(b)** MWCNT

Based on the device operation mechanism, CNFET can be classified as following, Schottky

Barrier CNFET (SB-CNFET), MOSFET-like FET and Band-to-band tunneling CNFET (T-CNFET).

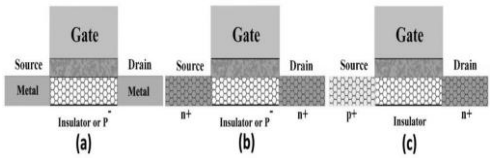


**Fig4 (a)** SB-CNFET,**(b)** MOS CNFET,**(c)**T-CNFET

### 2.2. LOGIC GATES

An Overview of Logic Gate

A digital Logic Gate is a basic device. Digital logic gates have more inputs but one digital output. [6, 8,9]. Logic gates are used to form combinational or sequential circuits, larger logic gate functions.

## III. LOGIC GATES

### 3.1 INVERTER

The inverter is the most basic of the logical gate. It has single input and single output. It inverts its input signal. The Boolean expression of inverter is : A=A'

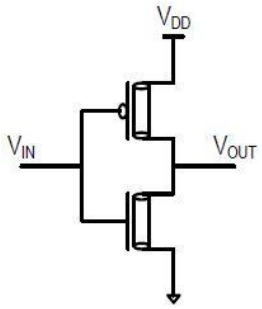


**Fig 5** Inverter

Inverter gates provide the complement of their input signal. When the input is '1' it produces the output as '0' and when the input is '0' the output is '1'.

### 3.2 AND GATE

The Boolean expression for AND Gate is A.B = Q. When the both inputs are high which provides high output otherwise which provides low output?

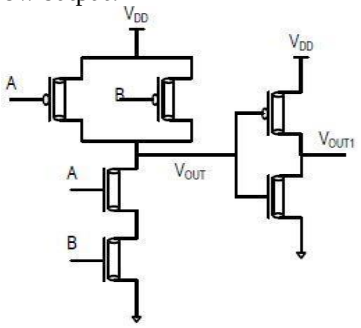


**Fig 6** AND Gate

### 3.3 NAND GATE

The Logic NAND Gate is created by combing the AND gate with an inverter in series. The NAND gate is the opposite form of the AND gate.

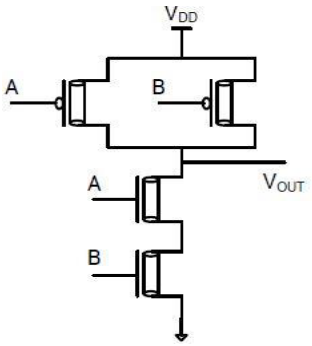


**Fig 7** NAND Gate

The Boolean expression for a NAND gate is A.B' =Q.

### 3.4 OR GATE

A OR Gate is also known as Inclusive – OR gate. When any one of the input is on then the output is on and when the both inputs are off the output also off.

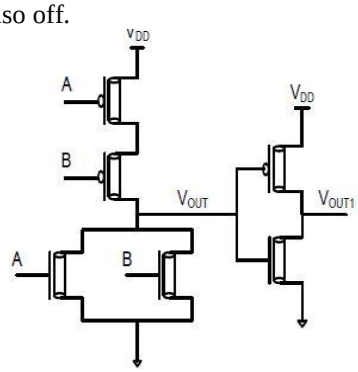


**Fig 8** OR Gate

The Boolean expression for OR gate is A+B=Q.

### 3.5 NOR GATE

The NOR Gate is formed by combining the OR gate and the inverter. It also known as Inclusive NOR gate.

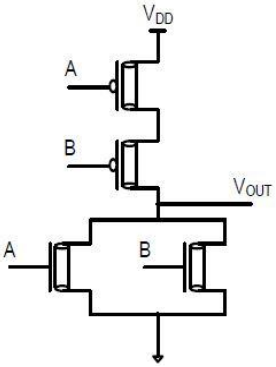


**Fig 9** NOR Gate

The Boolean expression for logic NOR gate is A+B'=Q.

# IV. ADDER CIRCUIT

## 4.1. INTRODUCTION TO ADDER

The adder is the digital circuit to perform addition in electronics [7, 10]. It is used to calculate addresses, table indices, and similar operations in processor [2]. Adders can be constructed for much numerical representation, such as binary-coded decimal. In cases where two's complement or one's complement is being used to represent negative numbers, it is trivial to modify an adder into an adder-subtractor. Other signed number representations require a more complex adder.

## 4.2. BLOCK DIAGRAM

A full adder can be implemented by composed of other gates. One example implementation is with S = A xor B xor Cin and Cout = (A.B) + (A xor B)). A full adder can be constructed by connecting two half adder. A and B to the input of first half adder, connecting the sum from that to an input to the second adder , connecting C as other input and OR the two carry outputs. The logic function of a 1-bit Full Adder cell with A, B, Cin (input carry) inputs and Sum and Cout (output carry) outputs are given in the following equations, in which _ symbol denotes the XNOR function:

$$Sum = XOR(A, B, C_{in}) = A.B.C_{in} + A.\overline{B}.\overline{C_{in}} + \overline{A}.B.\overline{C_{in}} + \overline{A}.\overline{B}.C_{in}$$
$$= A.(B \odot C) + B.(A \odot C) + C.(A \odot B)$$

$$C_{out} = Majority(A, B, C_{in}) = A.B + A.C_{in} + B.C_{in}$$

# V. ALU

The ALU is the important part of the Central Processing unit in computers. It performs operations such as addition, subtraction and multiplication of integers and bit-wise AND, OR, NOT, XOR and other Boolean operations.

## 5.1. INPUT OF ALU

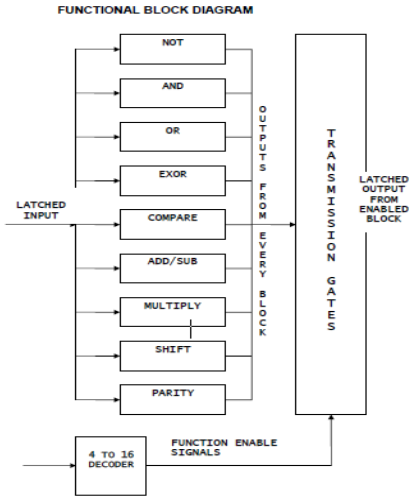


**Fig 10** Input Waveform for ALU

Input and the output waveforms are shown in Figure 10, 11 and Figure 12 respectively for ALU circuit. The proposed ALU circuit has 2 inputs, one carry input and 3 select lines. The resulted output is functional output and Carry out. The Figure 10explains about 2 inputs and carry input which are A, B, Cin waveforms.

## 5.2. OUTPUT OF ALU

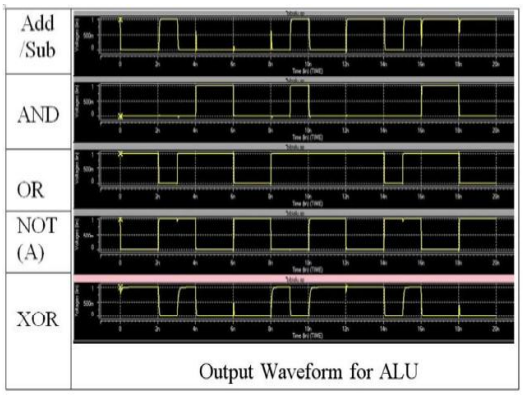


**Fig 11** Output waveform for ALU

The above Figure 11 shows the output waveforms for Adder/ Subtractor, AND, OR, NOT A, XOR .The output waveform of Comparator is shown in Figure 12. The first waveform is the output for less than value (A<B). The second waveform shows that the output for greater than values (A>B). The third waveform is the output for equal values (A=B) and the carry output cout.

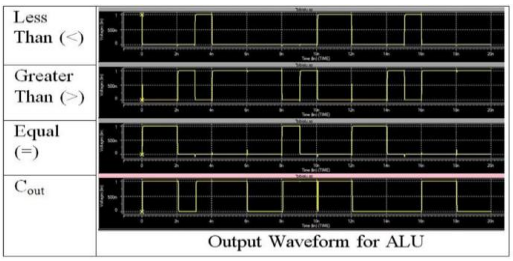


**Fig 12** Output waveform for ALU

The power dissipation in each sub-circuit of ALU is exhibited in Figure 7.Initially, the power dissipation of first sub-circuit is 176 n watts. Similarly the power dissipation has been calculated from all the sub-circuits. The total voltage source power dissipation calculated is 219.733n watts.

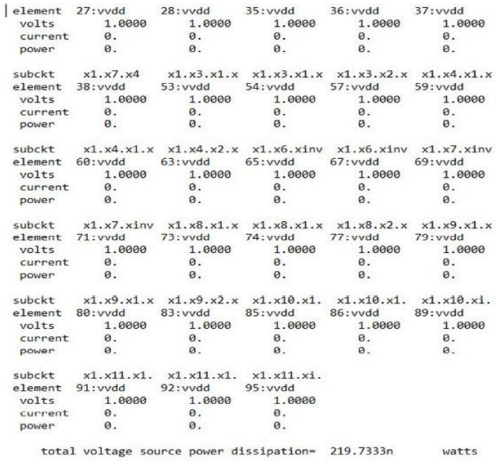


**Fig 13** Power Analysis from Netlist

## VI. CONCLUSION

This project presents designing of ALU using CNFET 32qnm technology. To minimize the leakage power, leakage current and operating power of a ALU CNFET technique has been employed. It is realized from the power analysis of ALU circuit as shown in Figure 13, the leakage power is found to be 219.733 nW. The HPICE EDA tool is used to get the simulation results. A reliable future work can be carried out in designing 4-bit ALU and other complex processing circuits using this ALU.

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